# A new proposed topology of 51 level Multi level Inverter with Reduced number of components

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***Abstract*-In this paper a new basic unit is proposed for multilevel inverters. The proposed basic units are used as building blocks to form a cascaded multilevel inverter i.e. the proposed topology consists of cascaded basic units and it uses lower number of switching devices and gate driver circuits. The design of proposed topology consists of mainly two parameters: the number of cascaded basic units and the number of dc sources in each basic unit. These two parameters can be used to design the desired multilevel inverter based on the operational conditions. Therefore the proposed topology offers good flexibility in designing. The comparison results with some recently introduced topologies showed that the proposed topology effectively reduces the components count. The simulation results obtained in MATLAB /SIMULINK as well as the experimental results of a 51-level inverter are presented and verified its performance.**

**Keywords:** THD, Multi-Level Inverter, IGBT & RES.

## I. INTRODUCTION

Multilevel inverters have found their place in medium-voltage high-power applications such as electric motor drives, flexible ac transmission systems and static VAR compensators [2–5]. The desired multi-staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra-capacitors are the most common independent sources used. Multilevel inverters generate stepped output voltage by a proper arrangement of power electronic switches and several dc voltage sources. As the number of output voltage levels increases, the output voltage becomes more identical to a sinusoidal waveform resulting in lower distortions. Multilevel inverters have some advantages in comparison with the conventional two-level inverters including the use of low-voltage power electronic switches and improved output voltage quality. This results in the lower stress on the power electronic devices and lower losses [6, 7].

Various circuit topologies are available for multilevel inverters. The conventional topologies are divided into three main types: the neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) multilevel inverters [8-13]. The NPC multilevel inverters have the problem of balancing the voltage of capacitors for higher number of voltage levels. Also, they need considerable number of clamping diodes. Therefore this type of multilevel inverters is limited to three-level case [14]. The FC multilevel inverter and it derivative topology stacked multi cell multilevel inverter use FCs to produce the voltage levels [15,16]. These inverters have the ability of self-balancing of the capacitors so that they can be extended to higher number of output voltage levels easier than the NPC inverters [17,18]. However, the FC inverters need high number of FCs for higher number of output voltage levels. The CHB multilevel inverters do not need clamping diodes and FCs. However, they need multiple isolated dc voltage sources [19]. CHB multilevel inverters can be divided to symmetric and asymmetric topologies from the view point of values of the dc voltage sources. In the symmetric topologies, the values of all of the dc voltage sources are equal. These topologies have good modularity and share the voltage stress on the switches in the same way. However, they need very high number of components as the number of voltage levels increases. On the other hand, in all of the asymmetric topologies [20,21] (including the proposed topology), the switches experience different stress. However, they use extremely lower number of components for a specific number of voltage levels. In this, a new cascaded asymmetric multilevel inverter is proposed. Firstly, a basic unit is proposed for the asymmetric multilevel inverter and then k basic units are cascaded to form the proposed asymmetric multilevel inverter. The proposed topology uses lower number of power electronic switches and gate driver circuits. In the next section the proposed topology and the algorithm for determining the values of dc voltage sources are described and then a comparison is presented. The simulation and experimental results of a 51-level inverter based on the proposed topology are presented to verify the capabilities of the topology.

## II. PROPOSED TOPOLOGY OF 51-LEVEL INVERTER

The proposed multilevel inverter uses series connected basic units. The Proposed basic unit for the multilevel inverter is shown in Fig.2.1. The basic unit is a combination of two parts which are connected to each other by two switches SP and SN. Each part of the basic unit consists of n/2 dc voltage sources, two unidirectional switches and n/2 – 1 bidirectional switches. Such a two-part arrangement for the basic unit allows increasing the number of voltage levels since dc voltage sources with different values can be used in the two parts. It is important to mention that generally in the asymmetric condition the main aim is to maximize the

number of voltage levels for a specific number of components. In all of the asymmetric topologies the modularity is lost and the switches do not share the operating voltage in the same manner. In other words, in all of the asymmetric topologies including the proposed topology, switches with different vo1ltage ratings are required. The unidirectional switches consist of an insulated gate bipolar transistor (IGBT) and its anti-parallel diode. The bidirectional switches consist of two IGBTs and their anti-parallel diodes connected in common-emitter form. The bidirectional switches experience bidirectional blocking voltage depending on the different switching combinations. Considering that the basic unit is composed of two parts, it uses n dc voltage sources, n − 2 bidirectional switches and six unidirectional switches. It is notable that the value of the dc voltage sources in each part of the basic unit are the same but the value of the dc voltage sources of the two parts can be different to generate more output voltage levels. To obtain the maximum number of output voltage levels, $V_2$ should be equal to the sum of all of the dc voltage sources with the value of V1 plus the value of one of them. In this way, there would be no redundant switching combination resulting in maximum number of voltage levels. Therefore the relation between the values of the dc voltage sources used in the two parts is as follows

$$V_2 = \frac{n}{2}V_1 + V_1$$
$$V_2 = (\frac{n}{2}+1)V_1 \quad \text{.... (1)}$$

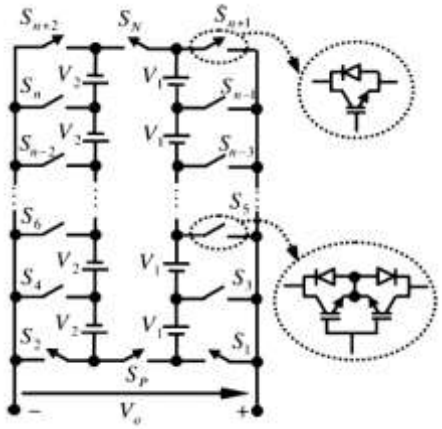

Fig.2.1 Proposed basic unit for multilevel inverter

It is important to note that in the proposed basic unit, both positive and negative voltage levels can be generated. For the positive voltage levels the switch SP is turned on and for the negative voltage levels the switch SN is turned on. Table.2.1 indicates the switching states of the proposed basic unit. Different output voltage levels can be generated according to this table. Although the proposed basic unit shown in Fig.2.1 uses bidirectional switches in addition to unidirectional switches, there are still some unidirectional switches that provide a path for current even if none of the switches are turned on. As the switches $S_1$, $S_2$, $S_p$ and the switches Sn + 1, Sn + 2, Sn are unidirectional, their diodes can conduct the current so that the current path is not disconnected anyway. In practice this condition can occur in dead time between the switches. The dead time is time delay between the switching commands of the switches to avoid short circuit. However, in the proposed topology, as there is always a path for current no extra stress is on the switches. As an example, considering (1), in the proposed basic unit with four dc voltage source (n = 4) the dc sources have the values of $V_1$, $V_1$, $3V_1$, $3V_1$ as shown in Fig.2.2 a. With these values for the dc voltage sources, the proposed basic unit produces a 17-level output voltage. Table.2.2 shows the output voltage of the 17-level converter in each switching state. The typical 17-level output voltage is shown in Fig.2.2 b.

To have more generality in the topology, the proposed basic units are cascaded to form a multilevel converter. The proposed multilevel converter consists of k basic units connected in series which is shown in Fig.2.3.

Table.2.1 switching states of proposed basic unit

| State | On switches | $v_o$ |
|---|---|---|
| 1 | $S_2, S_P, S_3$ | $V_1$ |
| 2 | $S_{n-1}, S_N, S_{n+2}$ | $-V_1$ |
| 3 | $S_2, S_P, S_5$ | $2V_1$ |
| 4 | $S_{n-3}, S_N, S_{n+2}$ | $-2V_1$ |
| ⋮ | ⋮ | ⋮ |
| $n-1$ | $S_2, S_P, S_{n+1}$ | $(n/2)V_1$ |
| $N$ | $S_1, S_N, S_{n+2}$ | $-(n/2)V_1$ |
| ⋮ | ⋮ | ⋮ |
| | $S_4, S_P, S_1$ | $V_2$ |
| | $S_n, S_N, S_{n+1}$ | $-V_2$ |
| | $S_6, S_P, S_3$ | $2V_2 + V_1$ |
| | $S_{n-1}, S_N, S_{n-2}$ | $-2V_2 - V_1$ |
| ⋮ | ⋮ | ⋮ |
| $(n/2+1)^2 - 1$ | $S_{n+2}, S_P, S_{n+1}$ | $(n/2)(V_1 + V_2)$ |
| $(n/2+1)^2$ | $S_1, S_N, S_2$ | $-(n/2)(V_1 + V_2)$ |
| $(n/2+1)^2 + 1$ | $(S_1, S_P, S_2)$ or $(S_{n+1}, S_N, S_{n+2})$ | 0 |

| State | On switches | $v_o$ |
|---|---|---|
| 1 | $(S_1, S_P, S_2)$ or $(S_5, S_N, S_6)$ | 0 |
| 2 | $S_2, S_P, S_3$ | $V_1$ |
| 3 | $S_2, S_P, S_5$ | $2V_1$ |
| 4 | $S_1, S_P, S_4$ | $3V_1$ |
| 5 | $S_3, S_P, S_4$ | $4V_1$ |
| 6 | $S_4, S_P, S_5$ | $5V_1$ |
| 7 | $S_1, S_P, S_6$ | $6V_1$ |
| 8 | $S_3, S_P, S_5$ | $7V_1$ |
| 9 | $S_5, S_P, S_6$ | $8V_1$ |
| 10 | $S_3, S_N, S_6$ | $-V_1$ |
| 11 | $S_1, S_N, S_6$ | $-2V_1$ |
| 12 | $S_4, S_N, S_5$ | $-3V_1$ |
| 13 | $S_3, S_N, S_4$ | $-4V_1$ |
| 14 | $S_1, S_N, S_4$ | $-5V_1$ |
| 15 | $S_2, S_N, S_5$ | $-6V_1$ |
| 16 | $S_2, S_N, S_3$ | $-7V_1$ |
| 17 | $S_2, S_N, S_1$ | $-8V_1$ |

Table.2.2 Switching states of the 17-level converter

**PROPOSED BASIC UNIT WITH FOUR DC VOLTAGE SOURCES FOR 17 LEVEL INVERTER:**

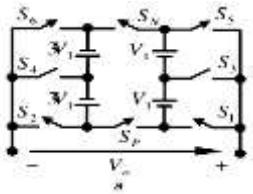

Fig.2.2 a 17-level basic unit based on the proposed topology

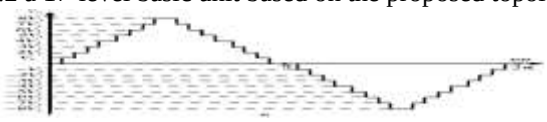

Fig.2.2 b Typical output voltage of the 17-level converter

## III. SIMULAIONA DIAGRAM & RESULTS

For verifying the proposed technology, the simulation and experimental results obtained for a 51-level inverter based on the proposed topology are presented. The simulation has been carried out for the circuit as shown in figure 3.1 in MATLAB SIMULINK environment. For experimentation, the gate signals pattern of the switches of the converter is given by Repeating sequence stair which provides the switching pulses. The switching pulses are applied to driver circuits that drive the switches. It is important to note that elimination of selected harmonics and total harmonic distortion (THD) minimization are not the aim of this project.

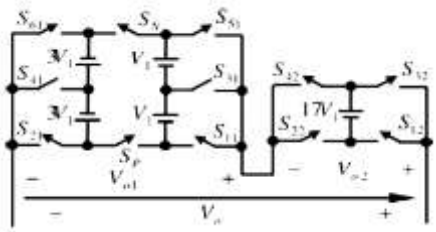

Fig.3.1 51-level converter based on the proposed topology with two cascaded basic units

**PROPOSED MATLAB MODEL OF 51 LEVEL INVERTER**

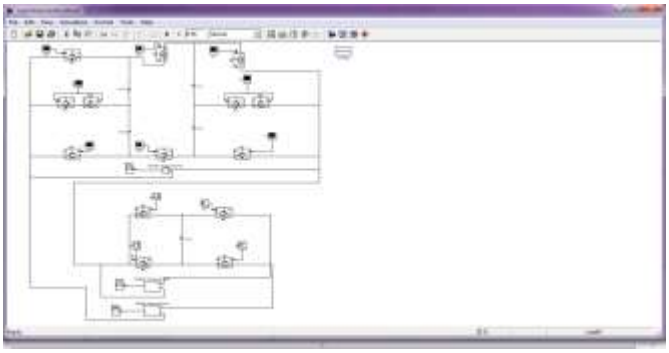

Fig.3.2 Simulation Diagram for proposed Circuit

**SWITCHING SEQUENCE FOR 51 LEVEL INVERTER:**

| S. NO | voltage | S1 | S2 | S3 | S4 | S5 | S6 | SP | SN | SA | SB | SC | SD |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 2 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 2 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 4 | 3 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 5 | 4 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 6 | 5 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 7 | 6 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 8 | 7 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 9 | 8 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 10 | 9 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 11 | 10 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 12 | 11 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 13 | 12 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 14 | 13 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 15 | 14 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 16 | 15 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 17 | 16 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 18 | 17 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 19 | 18 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 20 | 19 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 21 | 20 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 22 | 21 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 23 | 22 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 24 | 23 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 25 | 24 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 26 | 25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | -9 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 11 | -10 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 12 | -11 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 13 | -12 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 14 | -13 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 15 | -14 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 16 | -15 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 17 | -16 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 18 | -17 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 19 | -18 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 20 | -19 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 21 | -20 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 22 | -21 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 23 | -22 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 24 | -23 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 25 | -24 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 26 | -25 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

The 51-level converter based on the proposed topology uses 12 switches (and 12 gate driver circuits), 14 IGBTs and 5 dc voltage sources. The simulation results are shown in Fig.3.2. The output voltage of the first unit (vo,1) and second unit (vo,2) are shown in Figs.3.2 a and 3.2 b, respectively. Sum of these voltages is the total output voltage which is shown in Fig.3.2 c. As this figure shows the proposed multilevel converter can generate all of the expected levels of voltage.

| S. NO | voltage | S1 | S2 | S3 | S4 | S5 | S6 | SP | SN | SA | SB | SC | SD |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 2 | -1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 3 | -2 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 4 | -3 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 5 | -4 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 6 | -5 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 7 | -6 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 8 | -7 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 9 | -8 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

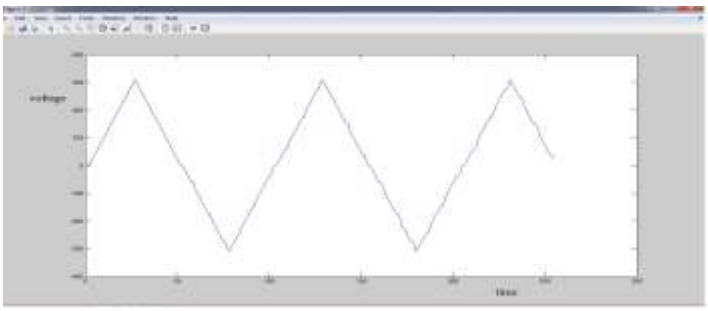

Fig 3.3 a Simulation Result of Output voltage without Load

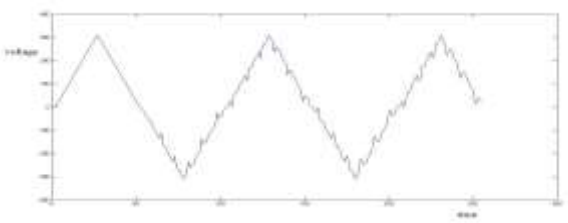

Fig.3.3 b Simulation result of Output voltage with Resistive load

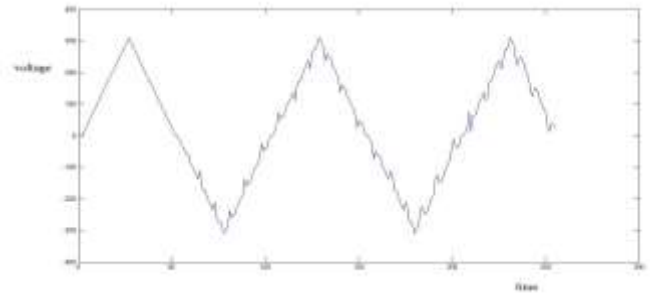

Fig.3.3 c Simulation result of Output voltage with Resistive-Inductive load

Fig.3.4 FFT Analysis of the output waveform

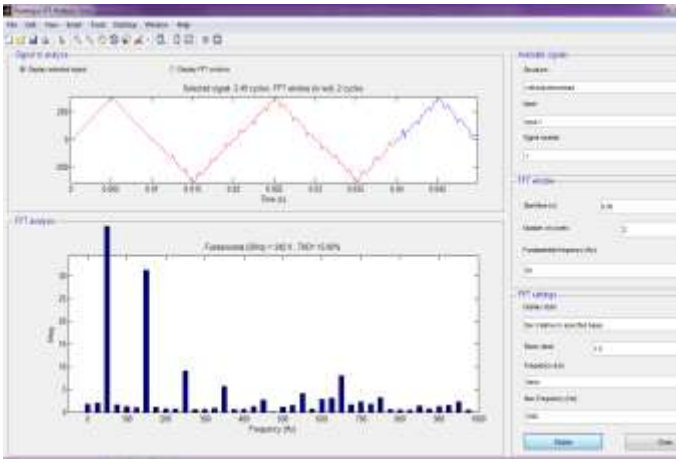

Fig.3.5 FFT analysis of output

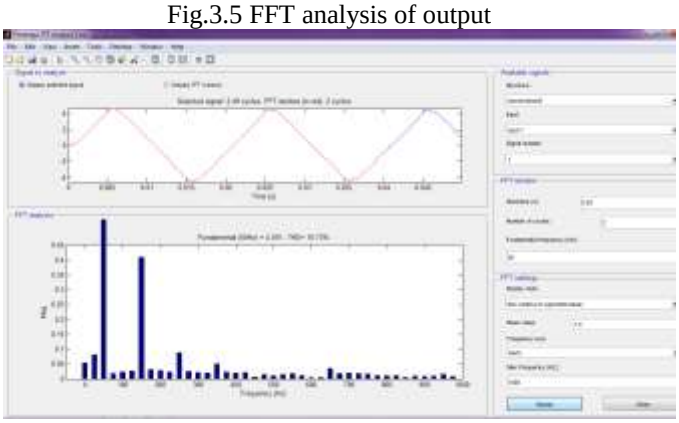

Fig.3.5 FFT analysis of output current

## CONCLUSION

As the presented topology consists of the cascaded basic units. The proposed basic unit and the proposed multilevel inverter uses lower number of switching devices and gate driver circuits, the proposed topology considers two design parameters. They are the number of cascaded basic units and the number of dc voltage sources in each basic unit. These two parameters can be used to design the desired multilevel converter based on the operational conditions. Thus the proposed topology offers good flexibility in designing. The simulation results obtained in MATLAB/Simulink as well as the experimental results of a 51-level Inverter based on the proposed topology are presented to verify its performance. Multilevel Inverters generate stepped output voltage by a proper arrangement of power electronic switches and several dc voltage sources. As the number of output voltage levels increases, the output voltage becomes more identical to a sinusoidal waveform resulting in lower distortions. Multilevel Inverters have some advantages in comparison with the conventional two-level Inverters and the other previous proposed topologies including the use of low-voltage power electronic switches and improved output voltage quality. This results in the lower stress on the power electronic devices and lower losses. The results have been presented and analyzed.

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